Quick filter Implementation for SPI:

Pins required:

1. DRDY signal to be generated by slave
2. SSn signal is generated by Master
3. CS general pin for slave
4. Sclk
5. SO
6. SI (will define the mode of operation)

Requirements:

1. What is the Run mode for SPI (is it similar to Quick filter, in Quick Filter Run mode, typically sends zeros i.e from master (SI pin)?
2. Control logic (SYNC logic) to select the channels from SPI?
3. SPI\_CTRL (Fast\_ch) required or not (this is for monitoring DRDY signal in Quick Filter)?
4. Size of the output register is 80 bits for the master to access data?
5. Is a Flag byte or Header byte required?
6. What is the Control logic for reading the data from 80 bits and the number of control registers are required?
7. S12SPIV4 from Motorola used.
8. 3 modes in the SPI namely Wait, Stop and Run mode.

Flowchart: -

No

Yes

No

Write FIFO (of selected channel)

Is Multichannel?

Set proper value

Check SPI\_CTRL Register

Latch DRDY signal

and

generate Interrupt

Master would control SSn pin and would generate sclk

Set DRDY signal High (Calculate the highest Fs)

Set enableReg (8 bit register for selecting channel after its processed by FIR filter)

nChannels, Fs

No FIFO write

FIFO Write

Is New data?

Generate Clk for Memory transfer

Write to shift register